TZA3012HW

30 Mbit/s up to 3.2 Gbit/s A-Rate fiber-optic receiver

Rev. 01 — 15 December 2005 Product data sheet

1. General description

The TZA3012HW is a fully integrated optical network receiver containing a dual limiter, data and clock recovery and demultiplexer with demultiplexing ratios of 1 : 16, 1 : 10, 1 : 8, or 1 : 4.

The A-rate feature allows the IC to operate at any bit rate between 30 Mbit/s and 3.2 Gbit/s using a single reference frequency. The receiver supports loop modes with serial clock and data inputs and outputs. All clock signals are generated using a fractional N synthesizer with 10 Hz resolution giving a true, continuous rate operation. For full configuration flexibility, the receiver can be configured by pin or via the I^2C-bus.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

2. Features

2.1 General

- Single 3.3 V supply voltage
- I^2C-bus and pin configured fiber-optic receiver

2.2 Dual limiter

- Dual limiting input with 12 mV sensitivity
- Received Signal Strength Indicator (RSSI)
- Loss-Of-Signal (LOS) indicator with threshold adjust
- Differential overvoltage protection

2.3 Data and clock recovery

- Supports SHD/SONET bit rates at 155.52 Mbit/s, 622.08 Mbit/s, 2488.32 Mbit/s and 2666.06 Mbit/s (STM16/OC48 + FEC)
- Supports Gigabit Ethernet at 1250 Mbit/s and 3125 Mbit/s
- Supports Fiber Channel at 1062.5 Mbit/s and 2125 Mbit/s
- ITU-T compliant jitter tolerance
- Frequency lock indicator
- Stable clock signal when input data absent
- Outputs for recovered data and clock loop mode

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2.4 Demultiplexer

- Demultiplexing ratios of 1 : 16, 1 : 10, 1 : 8 or 1 : 4
- Low Voltage Positive Emitter Coupled Logic (LVPECL) or Common Mode Logic (CML) demultiplexer outputs
- Parity bit generation
- Loop mode inputs to demultiplexer

2.5 Additional features with I^2C-bus

- A-rate supports any bit rate from 30 Mbit/s to 3.2 Gbit/s with one reference frequency
- Programmable frequency resolution of 10 Hz
- Four reference frequency ranges
- Adjustable swing of data, clock and parallel outputs
- Programmable polarity of all RF I/Os
- Exchangeable pin designations of RF clock with data for all I/Os for optimum connectivity
- Reversible pin designations of parallel data bus bits for optimum connectivity
- Slice level adjustment to improve Bit Error Rate (BER)
- Mute function for a forced logic 0 output state
- Programmable parity

3. Applications

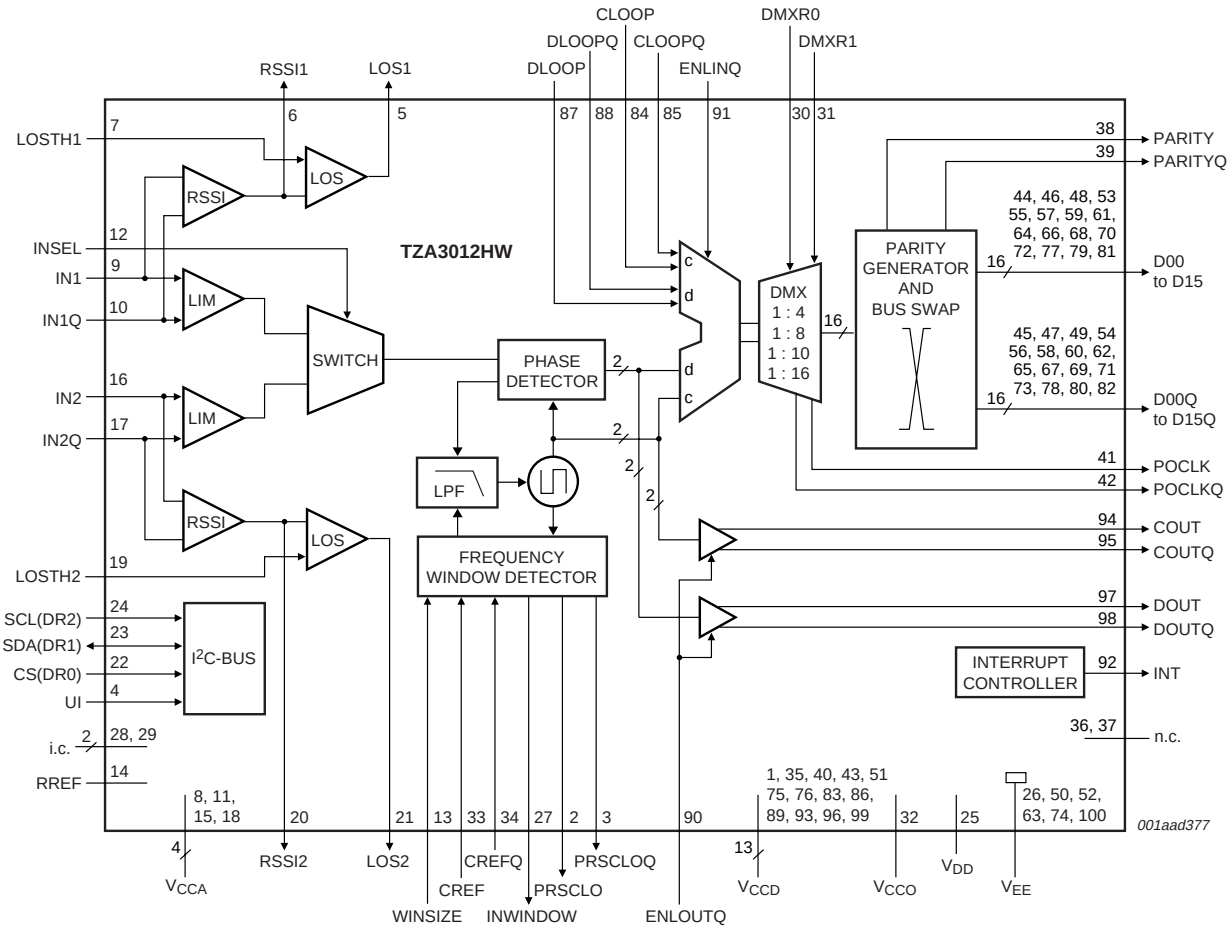
- Any optical transmission system with bit rates between 30 Mbit/s and 3.2 Gbit/s
- Physical interface IC in receive channels
- Transponder applications
- Dense Wavelength Division Multiplexing (DWDM) systems

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
TZA3012HW	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body 14 × 14 × 1 mm; exposed die pad	SOT638-1

5. Block diagram



LIM = Limiting amplifier

RSSI = Received signal strength indicator

LOS = Loss-of-signal detector

LPF = Low-pass filter

DMX = Demultiplexer

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

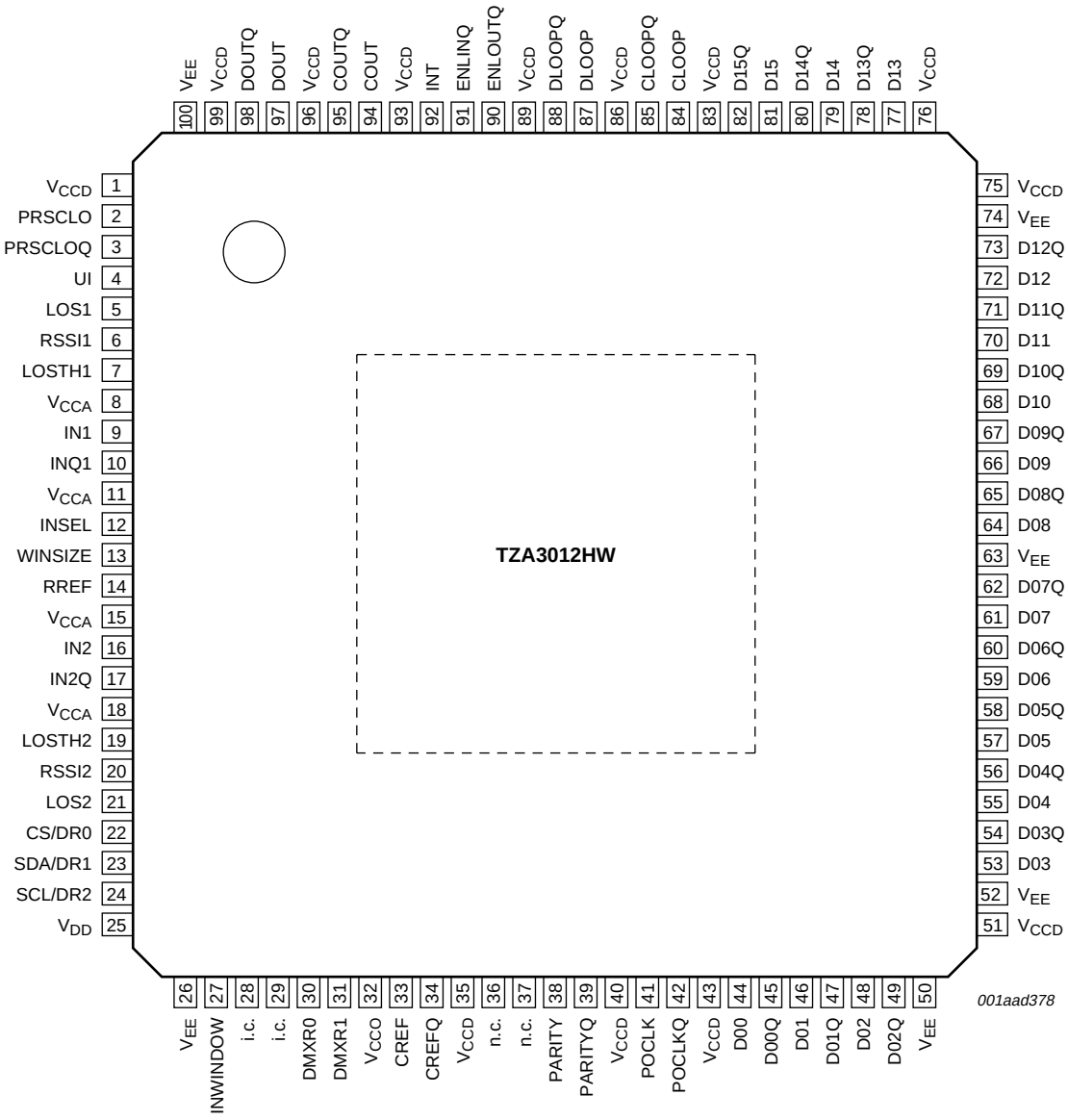


Fig 2. Pin configuration

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
V_{CCD}	1	supply voltage (digital signal part)
PRSCLO	2	prescaler output
PRSCLOQ	3	prescaler inverted output
UI	4	user interface select input
LOS1	5	first input channel loss-of-signal output
RSSI1	6	first input channel received signal strength indicator output
LOSTH1	7	first input channel loss-of-signal threshold input
V_{CCA}	8	supply voltage (analog part)
IN1	9	first channel input
IN1Q	10	first channel inverted input
V_{CCA}	11	supply voltage (analog part)
INSEL	12	input selector
WINSIZE	13	wide and narrow frequency detect window select input
RREF	14	reference resistor input
V_{CCA}	15	supply voltage (analog part)
IN2	16	second channel input
IN2Q	17	second channel inverted input
V_{CCA}	18	supply voltage (analog part)
LOSTH2	19	second input channel loss-of-signal threshold input
RSSI2	20	second input channel received signal strength indicator output
LOS2	21	second input channel loss-of-signal output
CS/DR0	22	chip select input or data rate select input 2
SDA/DR1	23	I^2C-bus serial data input and output or data rate select input 1
SCL/DR2	24	I^2C-bus serial clock input or data rate select input 2
V_{DD}	25	supply voltage (digital controller part)
V_{EE}	26	ground
INWINDOW	27	frequency window detector output
i.c.	28	internally connected; leave open
i.c.	29	internally connected; leave open
DMXR0	30	demultiplexing ratio select 0
DMXR1	31	demultiplexing ratio select 1
V_{CCO}	32	supply voltage (clock generator part)
CREF	33	reference clock input
CREFQ	34	reference clock inverted input
V_{CCD}	35	supply voltage (digital signal part)
n.c.	36	not connected
n.c.	37	not connected
PARITY	38	parity output
PARITYQ	39	parity inverted output

Table 2: Pin description *…continued*

Symbol	Pin	Description
V_{CCD}	40	supply voltage (digital signal part)
POCLK	41	parallel clock output
POCLKQ	42	parallel clock inverted output
V_{CCD}	43	supply voltage (digital signal part)
D00	44	parallel data 00 output
D00Q	45	parallel data 00 inverted output
D01	46	parallel data 01 output
D01Q	47	parallel data 01 inverted output
D02	48	parallel data 02 output
D02Q	49	parallel data 02 inverted output
V_{EE}	50	ground
V_{CCD}	51	supply voltage (digital signal part)
V_{EE}	52	ground
D03	53	parallel data 03 output
D03Q	54	parallel data 03 inverted output
D04	55	parallel data 04 output
D04Q	56	parallel data 04 inverted output
D05	57	parallel data 05 output
D05Q	58	parallel data 05 inverted output
D06	59	parallel data 06 output
D06Q	60	parallel data 06 inverted output
D07	61	parallel data 07 output
D07Q	62	parallel data 07 inverted output
V_{EE}	63	ground
D08	64	parallel data 08 output
D08Q	65	parallel data 08 inverted output
D09	66	parallel data 09 output
D09Q	67	parallel data 09 inverted output
D10	68	parallel data 10 output
D10Q	69	parallel data 10 inverted output
D11	70	parallel data 11 output
D11Q	71	parallel data 11 inverted output
D12	72	parallel data 12 output
D12Q	73	parallel data 12 inverted output
V_{EE}	74	ground
V_{CCD}	75	supply voltage (digital signal part)
V_{CCD}	76	supply voltage (digital signal part)
D13	77	parallel data 13 output
D13Q	78	parallel data 13 inverted output
D14	79	parallel data 14 output
D14Q	80	parallel data 14 inverted output

Table 2: Pin description *…continued*

Symbol	Pin	Description
D15	81	parallel data 15 output
D15Q	82	parallel data 15 inverted output
V_{CCD}	83	supply voltage (digital signal part)
CLOOP	84	loop mode clock input
CLOOPQ	85	loop mode clock inverted input
V_{CCD}	86	supply voltage (digital signal part)
DLOOP	87	loop mode data input
DLOOPQ	88	loop mode data inverted input
V_{CCD}	89	supply voltage (digital signal part)
ENLOUTQ	90	line loop back enable input (active LOW)
ENLINQ	91	diagnostic loop back enable input (active LOW)
INT	92	interrupt output
V_{CCD}	93	supply voltage (digital signal part)
COUT	94	recovered clock output
COUTQ	95	recovered clock inverted output
V_{CCD}	96	supply voltage (digital signal part)
DOUT	97	recovered data output
DOUTQ	98	recovered data inverted output
V_{CCD}	99	supply voltage (digital signal part)
V_{EE}	100	ground
V_{EE}	die pad	common ground plane

7. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	analog supply voltage		–0.5	+3.6	V
V_{CCD}	digital supply voltage		–0.5	+3.6	V
V_{CCO}	oscillator supply voltage		–0.5	+3.6	V
V_{DD}	supply voltage		–0.5	+3.6	V
V_n	voltage on pin n				
	D00 to D15, D00Q to D15Q, POCLK, POCLKQ, PARITY, PARITYQ, PRSCLO and PRSCLOQ		V_{CC} – 2.5	V_{CC} + 0.5	V
	LOSTH1, LOSTH2 and RREF		–0.5	V_{CC} + 0.5	V
	RSSI1 and RSSI2		–0.5	V_{CC} + 0.5	V
	UI, INSEL, WINSIZE, CS, SDA, SCL, DMXR0, DMXR1, ENLOUTQ and ENLINQ		–0.5	V_{CC} + 0.5	V
	LOS1, LOS2 and INWINDOW		–0.5	V_{CC} + 0.5	V
	INT		–0.5	V_{CC} + 0.5	V
$I_{I(n)}$	input current on pin n				
	IN1, IN1Q, IN2 and IN2Q		–30	+30	mA
	CREF, CREFQ, CLOOP, CLOOPQ, DLOOP and DLOOPQ		–20	+20	mA
	INT		–2	+2	mA
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	+125	°C
T_{stg}	storage temperature		–65	+150	°C

8. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1] [2]	16	K/W

[1] In compliance with JEDEC standards JESD 51-5 and JESD 51-7.

[2] Four-layer Printed-Circuit Board (PCB) in still air with 36 plated vias connected with the heatsink and the second and fourth layer in the PCB.

9. Characteristics

Table 5: Default measurement settings

All measurements are done with the default settings.

Parameter	Pin
Pin configured mode	UI = LOW
STM16/OC48	DR0 = LOW, DR1 = HIGH, DR2 = LOW
Limiter 1 active	INSEL = HIGH
Detect window 1000 ppm	WINSIZE = HIGH
Disabled DOUT and COUT	ENLOUTQ = HIGH
Disabled DLOOP and CLOOP	ENLINQ = HIGH
DMX ratio = 1 : 16	DMXR0 = HIGH, DMXR1 = HIGH
Reference frequency	CREF and CREFQ = 19.44 MHz
LOS2 switched off	LOSTH2 = not connected
D00 to D15 and D00Q to D15Q	not connected
PARITY, PARITYQ	not connected
POCLK, POCLKQ	not connected
PRSCLO and PRSCLOQ	not connected

Table 6: Supply characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies: pins V_{CCA}, V_{CCD}, V_{CCO}							
V_{CC}	supply voltage			3.14	3.30	3.47	V
I_{CCA}	analog supply current			15	20	27	mA
I_{CCD}	digital supply current			270	350	450	mA
I_{CCO}	oscillator supply current			20	25	33	mA
$I_{CC(tot)}$	total supply current		[1]	305	395	511	mA
Digital controller: pins V_{DD}							
V_{DD}	supply voltage			3.14	3.30	3.47	V
I_{DD}	supply current			0	0	1	mA
General							
P_{tot}	total power dissipation		[1]	0.96	1.3	1.77	W
Reference: pin RREF							
V_{ref}	reference voltage	10 kΩ to 20 kΩ to V_{EE}		1.17	1.21	1.26	V

[1] The total supply current and power dissipation are dependent on the IC setups such as swing and loop modes and termination conditions.

Table 7: Logic control input and output characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMOS input: pins UI, DR0, DR1, DR2, INSEL, WINSIZE, DMXR0, DMXR1, ENLOUTQ and ENLINQ						
V_{IL}	LOW-state input voltage		-	-	$0.2V_{CC}$	V
V_{IH}	HIGH-state input voltage		$0.8V_{CC}$	-	-	V
I_{IL}	LOW-state input current	V_{IL} = 0 V	−200	-	-	µA
I_{IH}	HIGH-state input current	$V_{IH} = V_{CC}$	-	-	10	µA
CMOS output: INWINDOW and INT						
V_{OL}	LOW-state output voltage	I_{OL} = 1 mA	0	-	0.2	V
V_{OH}	HIGH-state output voltage	I_{OH} = −0.5 mA	V_{CC} − 0.2	-	V_{CC}	V
Open-drain output: pin INT						
V_{OL}	LOW-state output voltage	I_{OL} = 1 mA	0	-	0.2	V
I_{OH}	HIGH-state output current	$V_{OH} = V_{CC}$	-	-	10	µA

Table 8: RF input, RSSI and LOS characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RF input: pins IN1, INQ1, IN2 and INQ2							
$V_{i(p-p)}$	peak-to-peak input voltage	single-ended	[1]	12	-	500	mV
$V_{sl(lower)}$	lower slice level voltage		[2]	-	−50	-	mV
$V_{sl(upper)}$	upper slice level voltage		[2]	-	+50	-	mV
Z_i	input impedance	differential		80	100	120	Ω
$\alpha_{isol(ch-ch)}$	isolation between channels			-	60	-	dB
RSSI circuit							
$V_{i(sens)}$	input sensitivity voltage	V_i = 5 mV to 500 mV (p-p)		15	17	20	mV/dB
Output: pins RSSI1 and RSSI2							
V_O	output voltage	V_i = 32 mV (p-p); PRBS = $(2^{31} - 1)$		580	680	780	mV
ΔV_O	output voltage variation	input 30 Mbit/s to 3200 Mbit/s; PRBS = $(2^{31} - 1)$; V_{CC} = 3.14 V to 3.47 V; ΔT_{amb} = 120 °C		−50	-	+50	mV
$I_{O(source)}$	output source current			-	-	1	mA
$I_{O(sink)}$	output sink current			-	-	0.4	mA
Z_o	output impedance			-	1	10	Ω
LOS detector							
LOS circuit							
$V_{hys(i)}$	input hysteresis voltage		[3]	-	3	-	dB
t_{as}	assert time	$\Delta V_{i(p-p)}$ = 3 dB		-	-	5	µs
t_{das}	de-assert time	$\Delta V_{i(p-p)}$ = 3 dB		-	-	5	µs

Table 8: RF input, RSSI and LOS characteristics *…continued*

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)}$ ≤ 16 K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMOS output: pins LOS1 and LOS2						
V_{OL}	LOW-state output voltage	I_{OL} = 1 mA	0	-	0.2	V
V_{OH}	HIGH-state output voltage	I_{OH} = −0.5 mA	V_{CC} − 0.2	-	V_{CC}	V

[1] The RF input is protected against a differential overvoltage; the maximum input current is 30 mA. It is assumed that both inputs carry a complementary signal of the specified peak-to-peak value.

[2] The slice level is adjustable in 256 steps controlled by I²C-bus registers LIMSLICE1 (address C0h) and LIMSLICE2 (address C1h).

[3] The hysteresis is adjustable in 8 steps controlled by bits HYS1 and HYS2 in I²C-bus registers LIMLOS1CNF (address BDh) and LIMLOS2CNF (address BFh).

Table 9: Clock and PLL characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)}$ ≤ 16 K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reference input frequency: pins CREF and CREFQ						
$V_{i(p-p)}$	peak-to-peak input voltage	single-ended	50	-	1000	mV
V_I	input voltage		V_{CC} − 1	-	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
$f_{i(ref)}$	reference input frequency	R = 1, 2, 4 or 8	18R	19.4R	21R	MHz
$\Delta f_{i(ref)}$	reference input frequency accuracy	SDH/SONET requirement	−20	-	+20	ppm
PLL characteristics						
t_{acq}	acquisition time	30 Mbit/s	-	-	200	µs
$t_{acq(pc)}$	power cycle acquisition time	30 Mbit/s	-	-	10	ms
$t_{acq(oc)}$	octave change acquisition time	30 Mbit/s	-	-	10	µs
TDR_{max}	maximum transitionless data run	30 Mbit/s	-	1000	-	bit

Table 10: Serial input and output characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)}$ ≤ 16 K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

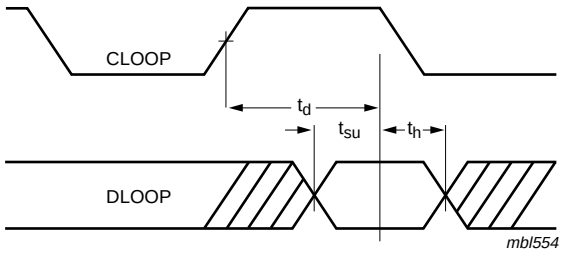
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial input: pins CLOOP, CLOOPQ, DLOOP and DLOOPQ						
$V_{i(p-p)}$	peak-to-peak input voltage	single-ended	50	-	100	mV
V_I	input voltage		V_{CC} − 1	-	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
t_d	delay time	data DLOOP and DLOOPQ to clock CLOOP and CLOOPQ; between differential crossovers referenced to negative clock edge	260	340	400	ps
t_{su}	setup time	see Figure 3	15	30	60	ps
t_h	hold time	see Figure 3	15	30	60	ps
δ_{clk}	clock duty cycle	clock CLOOP and CLOOPQ; between differential crossovers	40	50	60	%

Table 10: Serial input and output characteristics *...continued*

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Serial output: pins COUT, COUTQ, DOUT and DOUTQ							
$V_{o(p-p)}$	peak-to-peak output voltage	single-ended with 50 Ω external load; ENLOUTQ = LOW	[1]	50	80	110	mV
Z_o	output impedance	single-ended to V_{CC}		80	100	120	Ω
t_r	rise time	20 % to 80 %		-	100	-	ps
t_f	fall time	80 % to 20 %		-	100	-	ps
t_d	delay time	data DOUT and DOUTQ to clock COUT and COUTQ; between differential crossovers referenced to negative clock edge		80	140	200	ps
δ_{clk}	clock duty cycle	COUT and COUTQ; between differential crossovers		40	50	60	%

[1] The output swing is adjustable in 16 steps controlled by bits RFS in I^2C-bus register CBh.



The timing is measured from the crossover point of the clock input signal to the crossover point of the data input.

Fig 3. Loop mode input timing

Table 11: Parallel outputs characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Parallel output: pins D00 to D15, D00Q to D15Q, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ							
CML mode							
$V_{o(p-p)}$	peak-to-peak output voltage	single-ended with 50 Ω external load to V_{CC}; AC-coupled or DC-coupled	[1]	650	800	1000	mV
Z_o	output impedance	single-ended to V_{CC}		70	95	110	Ω
t_r	rise time	20 % to 80 %		200	250	350	ps
t_f	fall time	80 % to 20 %		200	250	350	ps
$f_{bit(par)}$	parallel bit rate			-	-	400	Mbit/s
LVPECL mode							
V_{OH}	HIGH-state output voltage	50 Ω termination to V_{CC} − 2 V		V_{CC} − 1.2	V_{CC} − 1.0	V_{CC} − 0.9	V
V_{OL}	LOW-state output voltage	50 Ω termination to V_{CC} − 2 V		V_{CC} − 2.0	V_{CC} − 1.9	V_{CC} − 1.7	V

Table 11: Parallel outputs characteristics *...continued*

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)}$ ≤ 16 K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{o(p-p)}$	peak-to-peak output voltage	LVPECL floating; single-ended with 50 Ω external load to V_{CC}; AC-coupled or DC-coupled	[1]	700	900	1150	mV
t_r	rise time	20 % to 80 %		300	350	400	ps
t_f	fall time	80 % to 20 %		300	350	400	ps
$f_{bit(par)}$	parallel bit rate			-	-	400	Mbit/s
Timing							
t_d	delay time	referenced to negative clock edge	[2]				
	data D00 to D15 to clock POCLK	DMX = 1 : 16, 1 : 10, 1 : 8		−100	+100	+250	ps
	data D06 to D09 to clock POCLK	DMX = 1 : 4		150	180	250	ps
δ_{clk}	clock duty cycle	POCLK and POCLKQ; between differential crossovers		40	50	60	%
$t_{sk(o)}$	output skew time	between channels	[2]				
	data D00 to data Dn	DMX = 1 : 16, 1 : 10, 1 : 8		-	-	200	ps
	data D06 to D09 to clock POCLK	DMX = 1 : 4		-	-	50	ps

[1] The output swing is adjustable in 16 steps controlled by bits MFS in I²C-bus register IOCNF3 (address C8h). In standard LVPECL mode only swing = 12 (default) should be used.

[2] With 50 % duty cycle.

Table 12: Jitter tolerance characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = −40 °C to +85 °C; $R_{th(j-a)}$ ≤ 16 K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{jit(tol)(p-p)}$	peak-to-peak jitter tolerance	ITU-T G.958; PRBS = $(2^{31} - 1)$	[1]				
		STM1/OC3 mode	[2]				
		f = 6.5 kHz		3	10	-	
		f = 65 kHz		0.3	1.0	-	
		f = 1 MHz		0.3	0.5	-	
		STM4/OC12 mode	[3]				
		f = 25 kHz		3	10	-	
		f = 250 kHz		0.3	1.0	-	
		f = 5 MHz		0.3	0.5	-	
		STM16/OC48 mode	[4]				
		f = 100 kHz		3	10	-	
		f = 1 MHz		0.3	1.0	-	
		f = 20 MHz		0.3	0.5	-	

[1] The peak-to-peak jitter tolerance is expressed as a ratio of the Unit Interval (UI):

$$t_{jit(tol)(p-p)} = \frac{UI(max) - UI(min)}{UI(nom)}$$

[2] The minimum value of the peak-to-peak jitter tolerance is 0.25 for T_{amb} = −40 °C to 0 °C at f = 65 kHz and 1 MHz.

[3] The minimum value of the peak-to-peak jitter tolerance is 0.25 for T_{amb} = –40 °C to 0 °C at f = 250 kHz and 5 MHz.

[4] The minimum value of the peak-to-peak jitter tolerance is 0.25 for T_{amb} = –40 °C to 0 °C at f = 1 MHz and 20 MHz.

Table 13: I²C-bus characteristics

V_{CC} = 3.14 V to 3.47 V; T_{amb} = –40 °C to +85 °C; $R_{th(j-a)}$ ≤ 16 K/W; all characteristics are specified for the default settings; all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC characteristics: pins SCL and SDA						
V_{IL}	LOW level input voltage		-	-	$0.2V_{CC}$	V
V_{IH}	HIGH level input voltage		$0.8V_{CC}$	-	-	V
V_{hys}	hysteresis of Schmitt trigger inputs		$0.05V_{CC}$	-	-	V
V_{OL1}	LOW level output voltage	SDA open-drain; I_{OL} = 3 mA	0	-	0.4	V
I_i	input current each I/O pin		–10	-	+10	µA
C_i	capacitance for each I/O pin		-	-	10	pF
C_b	capacitive load for each bus line		-	-	400	pF
V_{nL}	noise margin at the LOW-level		$0.1V_{CC}$	-	-	V
V_{nH}	noise margin at the HIGH-level		$0.2V_{CC}$	-	-	V
Timing (standard mode): pins SCL and SDA						
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
$t_{HD;DAT}$	data hold time		0	-	0.9	µs
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{SU;STO}$	setup time for STOP condition		0.6	-	-	µs
t_r	rise time of both SDA and SCL signals		20	-	300	ns
t_f	fall time of both SDA and SCL signals		20	-	300	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	-	50	ns

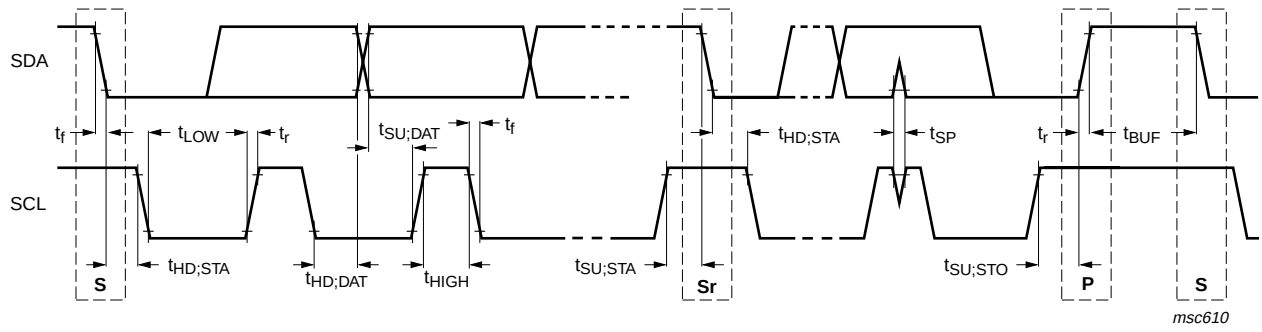
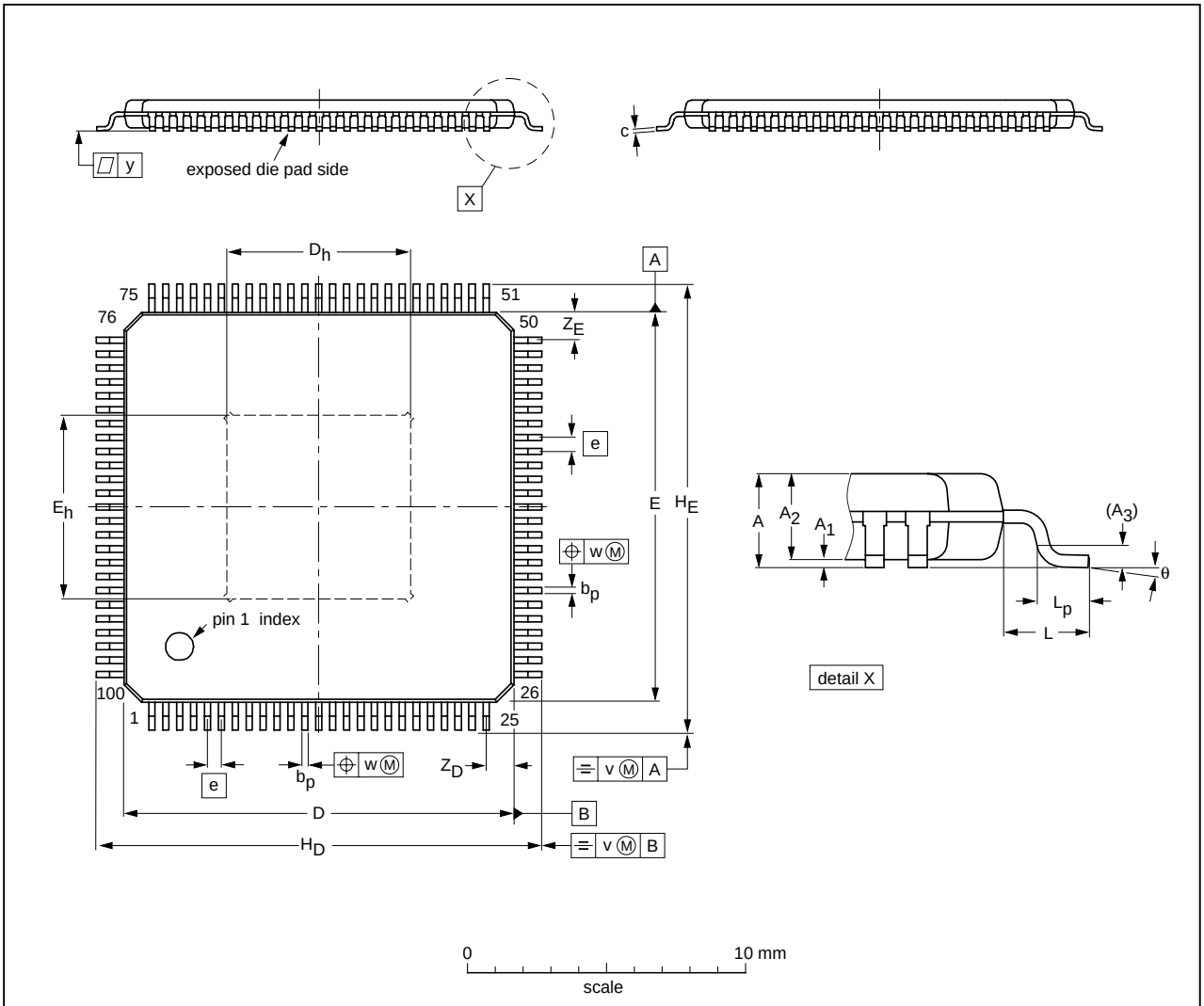


Fig 4. I²C-bus timing

10. Package outline

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad

SOT638-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1		MS-026				~~03-04-07~~ 05-02-02

Fig 5. Package outline SOT638-1 (HTQFP100)

11. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TZA3012HW_1	20051215	Product data sheet	-	-	-

12. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

13. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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17. Contents

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